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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/613,653	07/03/2003	Paul A. LaBerge	6909.01	7250

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EXAMINER	
SIEK, VUTHE	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 03/09/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/613,653	LABERGE, PAUL A.	
	Examiner	Art Unit	
	Vuthe Siek	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 January 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *20-28* is/are pending in the application.

4a) Of the above claim(s) *28* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *20-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/8/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application 10/613,653 and response to restriction/election requirement filed on 1/3/2006. The elected Claims 20-27 without traverse have been acknowledged and the non-elected claim 28 has been withdrawn. Applicant is requested to cancel claim 28 in the next communication.

2. **Notes**:

On 7/3/03, Applicant has filed Preliminary Amendment, claims 20-25 and 35-38 are canceled (page 3), where claims 26-34 remain pending (page 5). However, only claims 1-19 have been originally filed.

On August 10, 2005, Applicant has submitted a Preliminary Amendment having claims 20-38, where claims 1-19 are canceled.

In reply to a non-compliant dated 8/15/05, Applicant has filed on September 19, 2005, where claims 1-19 are canceled, and claims 20-28 remain pending. These claims 20-28 are the same set of claims 26-34 filed in August 10, 2005.

On September 30, 2005, claims 20-38 have been restricted (claims filed August 10, 2005), and the Restriction/Election has been mailed according to claims 20-38 filed in August 10, 2005.

On December 29, 2005, an interview was conducted initiated by Applicant regarding to restriction requirement (see interview summary page 5, filed 1/3/06). Due to previous restriction/election, claims 20-28 (same claims 26-34 filed August 10, 2005 that were restricted on September 30, 2005) are also restricted as indicated in the interviews summary per applicant dated January 3, 2006.

The file now is corrected as followed:

The statement that claims 20-25 and 35-38 are canceled (page 3) should be deleted (date file 7/3/03).

The Preliminary Amendment filed on August 10, 2005 should be invalid.

Claims 20-27 remain pending for examination, where **claim 28** is withdrawn due restriction. Applicant is requested to cancel claim 28 as non-elected claim.

Specification

3. The abstract filed on 9/19/05 is objected to because phrase "The Abstract and, ... MPEP 608.01(b)" should be deleted. Correction is required. See MPEP § 608.01(b).

4. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

Claim Objections

5. Claim 20 is objected to "the manufacturing" should be changed to --a manufacturing--, in order to minor informality.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

7. Claim 20 is rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The limitation "providing an in-process semiconductor wafer", "examining a complete specimen of the ASIC with metal one layer" and "forming a metal one layer on said in-process semiconductor wafer different from the metal layer one layer of the completed specimen to effect the desired changes" are found in the disclosure. All depending claims are also virtually rejected based on the rejection of base claim.

Double Patenting

8. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double

patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

9. Claims 20-27 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-10 of U.S. Patent No. 6,601,228; claims 1-13 of U.S. Paten No. 6,209,118. Although the conflicting claims are not identical, they are not patentably distinct from each other because as a whole the claims in the instant application and the patent claims refereed to a method for modifying a logic design of an ASIC having integrated circuit connection circuitry connecting a plurality of circuit and programmable circuits. Although, the patent claims do not recite examining a complete specimen of the ASIC, it would have been obvious to practitioners in the art to recognize that a thorough examination must be done before making any necessary modifications to the logic design by forming a metal layer and configuring the metal layer in order to provide a new logic design before manufacturing process.

Claim Rejections - 35 USC § 102

10. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States

only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

11. Claims 20, 21, 24 and 27 are rejected under 35 U.S.C. 102(e) as being anticipated by Fudanuki et al. (6,054,872).

12. As to claim 20, Fudanuki et al. teach a process for use in a manufacturing of application specific integrated circuits (ASIC) (Fig. 11, col. 13 lines 1-67; summary). The process comprises providing a semiconductor wafer 1 that lacks of metal one layer on which has been formed a plurality of circuits that comprises a logic design and at least one programmable circuit. Fig. 11 shows a semiconductor wafer comprising magacells (col. 13, 1-16) and dispersed all over the wafer gate array basic cells and standard cells used for design modifications or design changes (col. 13, lines 17-67). Various circuit change can be implemented only by changing the overlying wiring layers with no influence on the underlying patterns of the standard cells, so that turn around time can be shortened (col. 4, lines 23-46). Fig. 5A is a plan view showing patterns before wiring layers are formed in the pattern layout (col. 8 lines 23-26; col. 8 lines 39-41). This suggests that the wafer lacks of a metal one layer. Fudanuki et al. teach the arrangement of gate array basic cells and standard cells is for use in various circuit change (design modifications) (col. 4 lines 23-46; col. 5 lines 10-53) by changing overlying metal wiring layers (metal one layer) (col. 4 lines 23-46; col. 5 lines 10-26; col. 7 lines 1-16). Fudanuki et al. teach circuit change by forming intermediate buffers using basic cells (col. 7 line 50 to col. 8 line 6), where the basic cells are the cells on which a metal wiring layer is not formed (col. 8, lines 39-43). In order to perform a circuit change, circuit designers must examine a complete specimen of the ASIC with a metal

one layer because the complete examination would guide the circuit designers how to make necessary change to various metal layers and by forming of metal layers that are needed for desired changes. Since Fudanuki et al. dispersing or spreading mixed of standard cells and basic cells including primitive cell and basic cell, where primitive cell is a cell having metal layer formed on it and basic cell is cell that do not have metal layer formed on (col. 8 lines 19-43). Thus, Fudanuki et al. forming a metal one layer (basic cell) on the in-process semiconductor wafer different from the metal one layer of the complete specimen (primitive cell) to effect the desired changes. In addition, Fig. 10B shows forming metal layers including first metal layers, second metal layer and third metal layers (col. 12 description of Fig. 10B).

13. As to claim 21, at least Fig. 10B shows interconnections of hybrid standard cell architecture (col. 12 description of Fig. 10B) and Fig. 11 shows integrating a plurality of circuits (Fig. 13, col. 1-29) and hybrid standard cell architecture (programmable circuits) in a single integrated semiconductor wafer by integrated circuit connection circuitry. Although, the integrated circuit connection circuitry is not shown in the figure, it must be include in order to complete the overall interconnection to form a complete circuit design.

14. As to claim 24, Fudanuki et al. teach providing at least one general purpose logic blocks that comprises the at least one programmable circuit (col. 13, lines 1-29).

15. As to claim 27, Figs. 10A-10B and 11 show dispersing a plurality of general-purpose logic blocks on a wafer (col. 13, lines 1-29).

Claim Rejections - 35 USC § 103

16. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

17. Claims 22-23 and 25-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fudanuki et al. (6,054,872) in view of Levitt (5,787,012).

18. As to claims 22-23 and 26, Fudanuki et al. do not teach the single integrated circuit (ASIC) comprising at least one configuration register on the in-process semiconductor wafer. Levitt teaches an integrated circuit including a first metal layer with first layer identification signal writing circuitry connections to produce first metal layer circuit identification signals and a second metal layer second layer identification signal writing circuitry connections to produce second metal layer circuit identification signals. When design changes need only made at only a single metal layer, the circuit identification signal can be changed locally at that metal layer, thereby obviating design changes at an additional metal layer. This highly desirable functionality (providing a plurality of versions of a logic design) is achieved with simple and flexible electrical connections and minimal additional logic (col. 23-33). That is changing the value of signals at any single metal layer is sufficient to generate a desired circuit identification number for storage in an identification register (col. 3 lines 35-53). The identification register is located within the integrated circuit (Fig. 3). Integrating the identification register (configuration register) as taught by Levitt into the integrated circuit design as

taught by Fudanuki, a plurality of versions of integrated circuit design would have been generated as desired by simply by changing values of signals (configuration data for a programmable circuit) at any signal metal layer.

19. As to claim 25, it is a common practice to test a semiconductor wafer upon which the plurality of circuits have been interconnected by integrated circuit connection circuitry as shown in Fig. 11 in order to verify whether the changes or modifications metal layers are properly connected in order to provide a logic design as desired and within design specifications.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vuthe Siek whose telephone number is (571) 272-1906.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on (571) 272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

VUTHE SIEK
PRIMARY EXAMINER